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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WALTER, CRAIG E	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,900	KO ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *4 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-4 and 6 are pending in the application.

Claims 4 and 6 have been amended.

Claim 5 remains cancelled.

Claims 4 and 6 are rejected.

Claims 1-3 are allowed.

Response to Amendment

2. Applicant's amendments and arguments filed on 29 January 2007 in response to the office action mailed on 3 November 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 4, the phrase "the logical unit cell block information corresponding to N number of unit cell blocks" lack antecedent basis. More specifically, a plurality of logical unit cell block information is previously set forth within the claim (i.e. each unit tag table contains "different logical unit cell block information in the N+1 number of unit tag tables"), however the claim subsequently recites "the logical unit cell block information corresponding to N number of unit cell blocks". Which of the plurality of logical unit cell block information among the N+1 unit tag tables is being claimed here?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart et al. (US Patent 4,914,577), hereinafter Stewart.

As for claims 4 and 6, Stewart teaches a method for controlling a tag block, comprising:

initializing the tag block in a semiconductor memory device (Fig. 2, element 136 – the translation memory (i.e. tag block) stores tag block information to facilitate with the system's memory management functions. The tag block must be initialized prior to storing address translation data. Additionally, the tag block contains

N+1 tag tables (i.e. N=1); the 2 tables are illustrated as elements 136a and 136b– col. 16, line 59 through col. 17, line 41. Also note Steward specifically addresses the use of semiconductor components in computer systems col. 1, lines 14-25); and

performing a data access operation of the semiconductor memory device in response to a physical unit cell address outputted from the tag block sensing a logical cell block address, the physical unit cell address corresponding to N+1 number of unit cell blocks (Stewart teaches the tag block as receiving logical address information from the CPU in order to translate and output corresponding physical address information in col. 3, line 46 through col. 4, line 2),

wherein the initializing the tag block in a semiconductor memory device including:

nullifying the N+1 number of unit tag tables (the two tables are stored in a RAM which is a non-persistent, therefore the tables are cleared upon reboot (col. 3, lines 46-57 and col. 13, line 66 through col. 14, line 6)).

selecting all of N+1 number of unit tag tables (each of the two tables are selected prior to storing translation data – col. 15, line 46 through col. 16, line 17);

storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, the logical unit cell block information corresponding to N number of unit cell blocks (information required for the translation are stored in each of the

two tag table – col. 16, line 59 through col. 17, line 41. If it is stored in both (N+1), it is stored in 1 (N)).

As for claim 6, Steward teaches a method for a refresh operation of a semiconductor device including a cell area (Fig. 2, element 136) having N+1 number of unit cell tables (Fig. 2, elements 136a and 136b), each including M number of word lines which respectively are coupled to a plurality of unit cells (since the data stored within each table/block is stored within a RAM, each cell/block inherently must contain at least one word line to address the data). A tag block having N+1 (Fig. 136a and 136b) number of unit tag tables, for sensing a logical cell block address to output a physical unit cell address corresponding to N+1 number of unit cell blocks, each having M number of registers for sensing an update of data (again, the memory used to implement this translation scheme is an RAM, which must inherently contain word lines to address the data). Also note, the tables depicted in by elements 136a and 136b contain both cell tables (i.e. addresses 0 through 16383 as shown in Fig. 2, and tag block/information which is illustrated in Fig. 2 by elements 138a and 140a for example). In other words, the translation memory contains both the cell tables and tag tables. The method comprising:

nullifying the N+1 number of unit tag tables (the two tables are stored in a RAM which is a non-persistent, therefore the tables are cleared upon reboot (col. 3, lines 46-57 and col. 13, line 66 through col. 14, line 6)).

selecting all of N+1 number of unit tag tables (each of the two tables are selected prior to storing translation data – col. 15, line 46 through col. 16, line 17);

storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables (information required for the translation are stored in each of the two tag table – col. 16, line 59 through col. 17, line 41. If it is stored in both (N+1), it is stored in 1 (N)).

wherein the N number of unit cell blocks are corresponded to the logical cell block address and one unit cell block is added for accessing data with high speed (both element 136a and 136b correspond to addresses translated for the CPU, and both of these table are used specifically for high speed data operation, therefore N (i.e. 1) is used for high speed operations (col. 15, lines 25-45).

Response to Arguments

5. Applicant's arguments with respect to the art rejections as previously applied to claims 4 and 6 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained.

As for claims 4 and 6, Applicant asserts, "Stewart does not disclose, teach or suggest a tag block, having N+1 number of unit tag tables, for sensing a logical cell block address included in an inputted row address to output a physical unit cell address corresponding to N+1 number of unit cell blocks. Herein, the logical cell block address corresponds to N number of unit cell blocks, i.e., a specification of a semiconductor

memory device receiving the inputted row address, and the physical unit cell address corresponds to N+ 1 number of unit cell blocks substantially included in the semiconductor memory device for high speed data access. Stewart, however, does not disclose the physical unit cell address and the logic cell block address according to Applicant's claimed invention".

This argument however is not persuasive. Examiner maintains that Stewart does in fact teach a tag block, having N+1 number of unit tag tables, for sensing a logical cell block address included in an inputted row address to output a physical unit cell address corresponding to N+1 number of unit cell blocks. Referring again to Fig. 2, and col. 16, l. 59 through col. 17, l. 41; the tag block (Fig. 2, element 136) contains 2 tag tables (Fig. 2, elements 136a and 136b). Stewart's system utilizes the tag block to receive logical address information from the CPU in order to translate and output corresponding physical address information – see col. 3, l. 46 through col. 4, l. 2. The translation table is specifically used for purpose of translating logical to physical addresses for subunits (i.e. blocks) of his memory. Additionally note Stewart does in fact teach physical unit cell addresses and logic cell block addresses (each block is associated with logical and physical addresses which are resolved via the tag table) in col. 3, l. 46 through col. 4, l. 2.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

3-27-07